corallia
Hellenic Technology Clusters Initiative
Ελληνική Πρωτοβουλία Τεχνολογικών Συνεργατικών Σχηματισμών

INTERNSHIP DAY



@ THE PATRAS INNOHUB, May 15th, 2012

HELIC

Τρίτη 15 Μαΐου 2012

HELIC WHO is WHO [1]

What: Electronic Design Automation (EDA) software technologies for the semiconductor market.

Who: 2 Elec. Eng. founders (Y. Koutsoyannopoulos, S. Bantas), based on own research @ NTUA

When: Founded May 2000

Where: Headquarter in California, R&D Athens, sales Japan

Vision: "To build global awareness for quality, reliability and innovation"

Mission Statement: "Enable first-pass silicon and shorten development cycles of high-speed digital, analog RF and millimeter-wave ICs"

HELIC WHO is WHO [2]

Applied Technology: *Rapid electromagnetic synthesis* and *modeling* of on-chip passive devices, high-frequency interconnects, bondwires and package parasitics

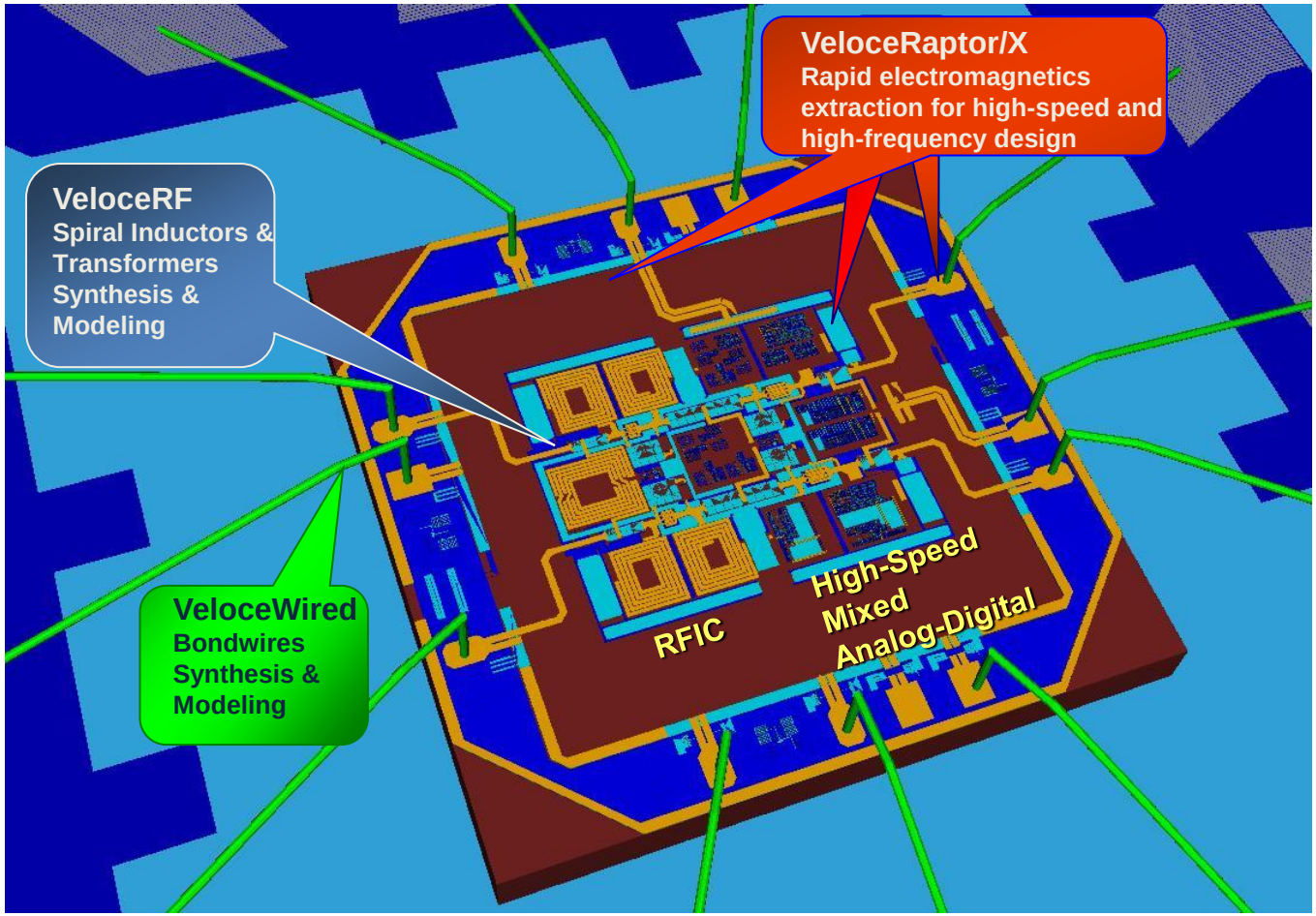
Data: Employees 5 @ 2001, 40 @ 2012 ◆ 100% export activity ◆ > 1000 circuit designers worldwide use Helic tools ◆ Customers: > 40 large semiconductor corporations

Success Story: Supplier of choice for Intel, Fujitsu, Freescale, Broadcom, Semiconductor, RF Micro Devices, Sony, AMD etc. ◆ 2008: Andy Bechtolscheim (founder of Sun Microsystems, first Google investor) becomes Helic investor

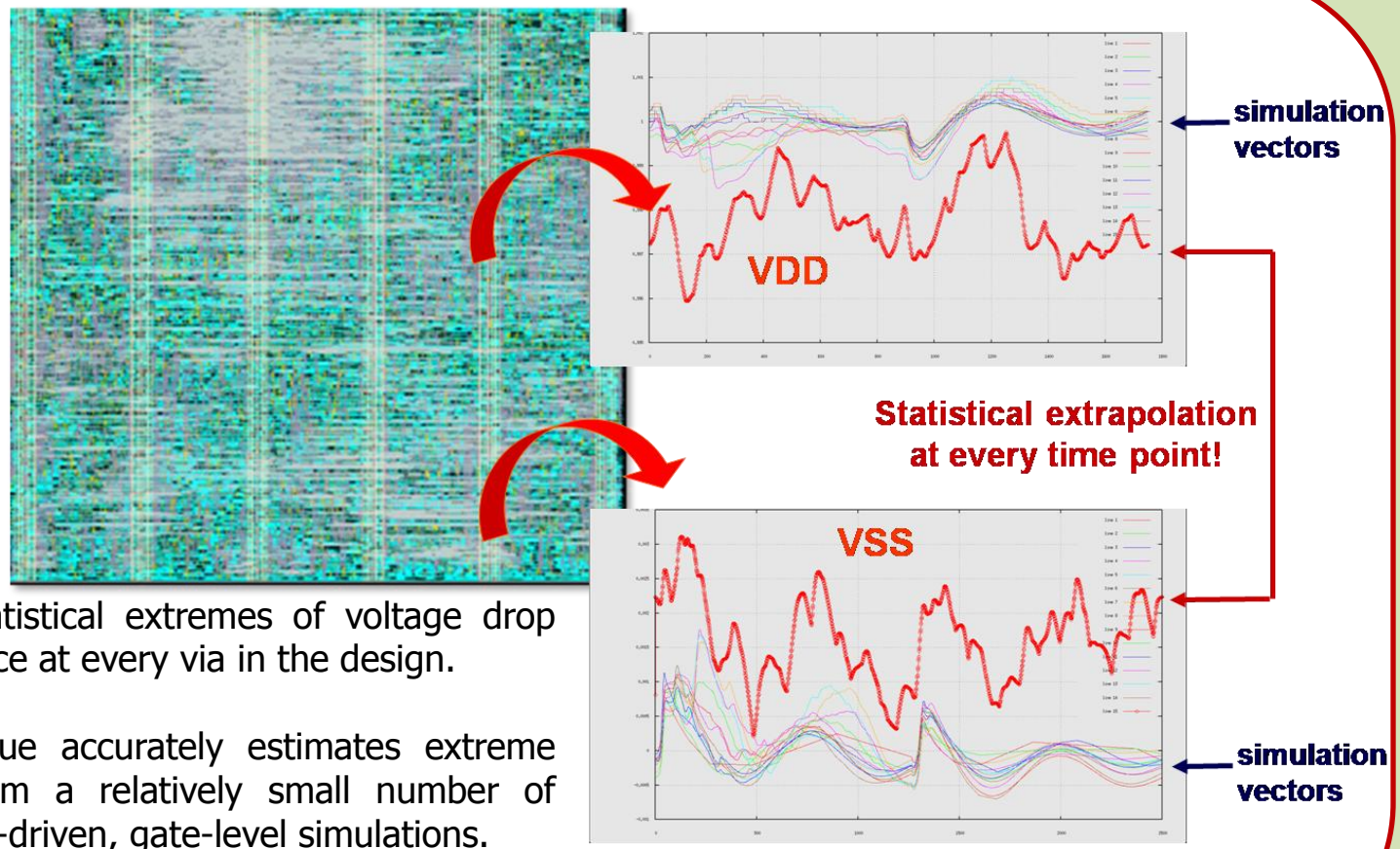
R&D orientation: Modeling for on-chip passives ◆ Electromagnetic simulation methods ◆ Tunable RF and microwave circuits ◆ Polygon Processing

In 5 years from now: New products (in progress) ◆ Customer base expansion in China and EU

VeloceRF, VeloceRaptor/X, VeloceWired
Analogue – Digital IC design



NanoPower
Lowering Barriers to Low Power



Estimation of statistical extremes of voltage drop and ground bounce at every via in the design.

Patented technique accurately estimates extreme voltage drop from a relatively small number of vector- or activity-driven, gate-level simulations.

Helps designers minimize power consumption

Internships

1. Research and development of algorithms suitable for 2D polygon processing and simplification
   C++, Polygon processing algorithms, Euclidean geometry

2. Verification flows for 20nm design
   C/C++, Microelectronics theory, Familiarity with Cadence

3. Parallel Computing for EDA applications
   C/C++, Parallel processing algorithms (grid/cloud).

4. Low power SoC design
   Good knowledge of digital design, VHDL programming skills, Familiarity with the digital design flow (from RTL to GDS)

5. 60 GHz Model Development for On-Chip Passives on Silicon
   Cadence Virtuoso, EM tools (ADS Momentum, Sonnet)

6. Capacitance Extraction for On-Chip Silicon Patterns
   Cadence Virtuoso, EM tools (ADS Momentum, Sonnet)

7. Administration: Cost accounting
   Cost accounting principles, Good knowledge of MS Excel

For more information visit: http://www.helic.com/forum