Analogies

Silicon Intellectual Property

Providing high-speed wired and wireless connectivity cores for SOC solutions

ANALOG INTEGRATED ELECTRONIC SYSTEMS

www.analogies.eu

EUROPEAN REGIONAL DEVELOPMENT FUND

COMPETITIVENESS AND ENTREPRENEURSHIP OPC II

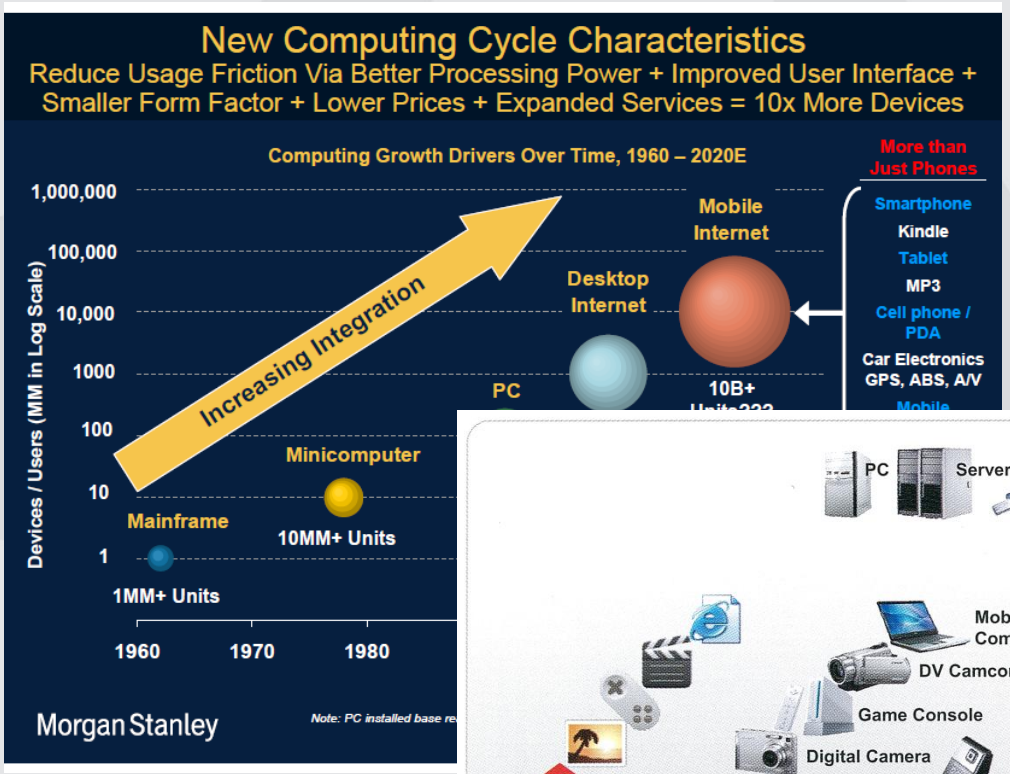
regions at the centre of development

(O.P. Competitiveness and Entrepreneurship (OPC II), O.P. Macedonia - Thrace, O.P. Western Greece - Peloponnesus - Ionian islands, O.P. Crete and Aegean islands, O.P. Thessaly - Mainland Greece - Epirus & O.P. Attica)

Overview

- Development and provision of high-speed wired and wireless connectivity intellectual property cores
- To serve fabless IC, IDMs, OEMs, ODMs designing SOCs that require high speed connectivity
- SOC developers have to cope with shrinking Time to Market windows, difficult to develop connectivity IP, elevated risk of failure
- We work to offer silicon proven, high speed interface cores, tailored to customer needs, providing time to market and risk mitigation
- Memory interface (DDR2/3), Wired (USB3) and Wireless (PLL), FEC (LDPC) IP cores - two alpha customer engagements
- To provide Per Use License IP, Design Service and IP Derivatives, direct in US and EU, via reps in Japan/APAC
- Strong management team, talented development team, experienced BoD
- Financially stable: founded 2006, has seed and startup capital of 1,85 m€ provided by the founders and a private equity firm – funds complimented by 2,36m€ of EU and Greek state grants - break even expected in 2013
- Working to establish its position into the silicon intellectual property market

Market Drivers



Source: Morgan Stanley De

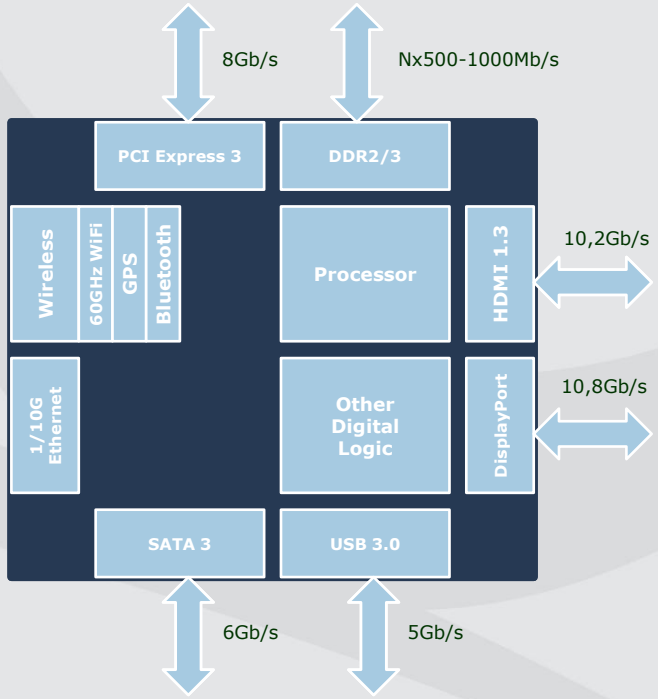
Proliferation of digital content and mobility

- Increasing bandwidth requirements drive need for high speed data transport interfaces
- Low standby and operating power at optimized performance

Next billion $ opportunities

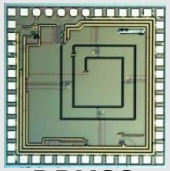
The Pain

- SOCs increasing in complexity and cost
  - Difficult to develop all IP blocks
  - Shrinking time to market window
  - Continued integration critical
- Growing Demand for Reusable & Proven IP
  - Difficult and costly to develop in-house
  - 2008: AVG SOC revenue 9.1m $,12m window,
    a 6 months slip costs 4,5m $ revenue*
  - IP licensing speeds time to market, reduces overall development expense, minimizes risk
- New Gigabit High Speed Interfaces
  - Far from trivial, require cross functional expertise
    to develop
  - High performance **and** low power

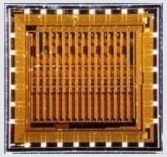


Products

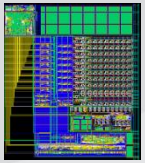
- **Very high speed PLL/VCO IPs, incl. patented distributed differential architecture**
  Working towards a 60GHz PLL, 14GHz DDVCO prototype available
  Technology applicable in 60GHz UWB/WirelessHD RF applications, as well as 77/79GHz Automotive Radar and Ultra High Speed Interfaces (40/100Gbit/s Ethernet)


DDVCO

- **Direct implementation of computational intensive signal processing functions for advanced iterative turbo-like forward error correction (FEC)**
  Currently as Analog SISO decoder prototype (ASISOD)
  In development of digital soft IP high throughput TURBO/LDPC codec, suitable for LTE backhaul, Mobile WiMAX, P1901 BPL, DVB-S2/RCS applications


ASISOD

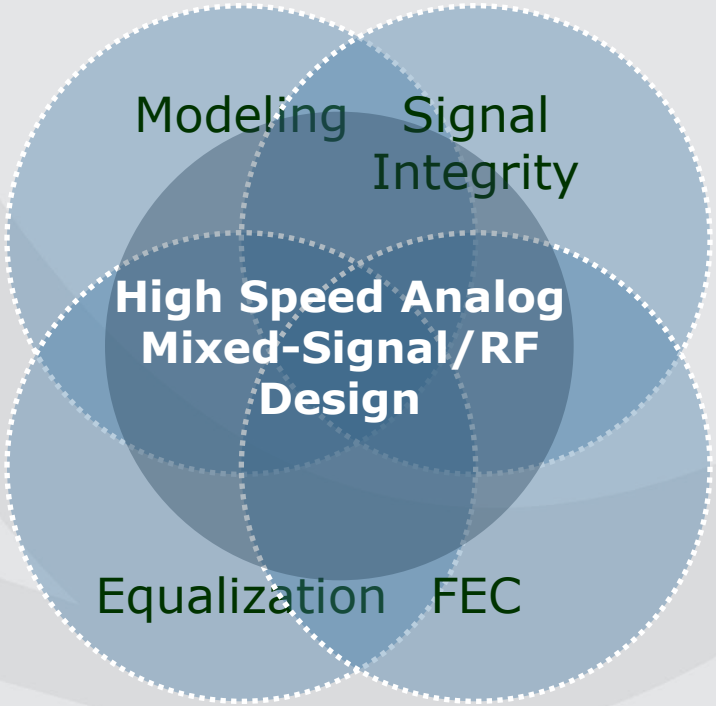
- **High Speed DDR2 SDRAM PHY with DFI compliant interface to memory controller, capable of up to 533MHz operating frequency**
  B0 prototype with interface to DFI Memory Controller consisting of soft and hard IP blocks, in TSMC 90nm available


DDR2PHY_B0

- **Superspeed USB3.0 PHY**
  Currently in early development phase for A0 prototype, to include soft and hard IP blocks, 8-16bit PIPE interface, in TSMC 65nm LP

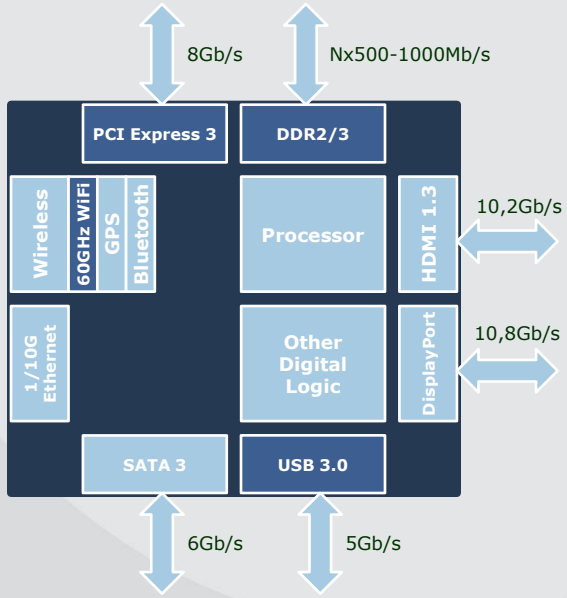
Technology

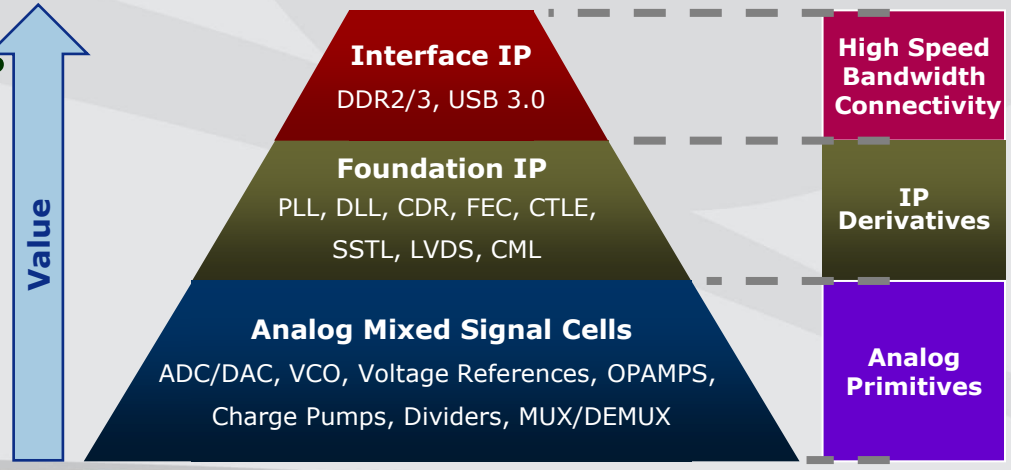
- Unique mix of algorithm modeling, signal integrity, equalization and forward error correction know how
- Advanced analog mixed-signal/RF design expertise
- Differentiated patent protected analog building cells (VCO, ADC, VREF, CP, FEC)
- High Performance **and** Low Power



Development Method

- Analog mixed-signal/RF High Speed Intellectual Property (IP) Interface Cores
  - Silicon proven for risk mitigation and time to market
  - Built from scratch for 90nm and less
  - Protected by patents
- Analog/mixed signal/RF integration design services
  - Customization to customer requirements
  - Derivative designs

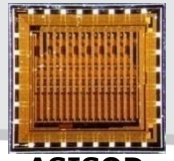


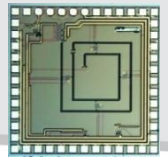


Timeline

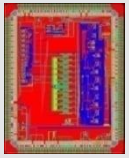
Q1-Q2 2006
Feasibility
Q2 2007
Operations

Q3 2006
Technology Prototypes


ASISOD


DDVCO

Q2 2008
DDR2 PHY A0

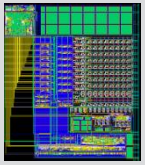

DDR2PHY_A0

Q1 2009
First Customer
Engagement

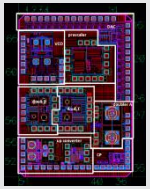
Q4 2008
LDPC FEC Core

Q1 2010 Analog
Mixed Signal Cells
Foundation Library

Q3 2009
B0 DDR2 PHY


DDR2PHY_B0

Q3 2010
HS LDPC FEC Core



Q3 2010
60GHz PLL
Test TO

Q3 2011
USB3.0 PHY
A0 TO

Q2 2011
60GHz PLL A0

Q4 2011
Gigabit LDPC

Advanced Design Tools & Infrastructure

- **Rich Analog/Mixed-signal (AMS) Design Flow Environment**
  - **Cadence Virtuoso Custom Design Platform** for analog/mixed-signal (AMS) design flow at **XL-level** including **Virtuoso Digital Implementation Option**
  - **Mentor Graphics'** AMS Unified SoC flow incl. **Calibre** for DRC/LVS
  - **Synopsys** digital implementation flow including back-end, consisting of VHDL and Verilog HDL, Power & DFT, PrimeRail & Formality, IC Compiler, DC Ultra and DesignWare Library
  - **Advanced RF and Microwave IC design** through **Ansoft's Designer, HFSS, Nexxim** and **Ansoftlinks** tools
  - **Mathworks Matlab and Ansoft Designer** for algorithmic/system modelling
- **BERTScope S 12500B 0.1—12.5 Gbps Signal Integrity Analyzer with Stressed Eye" from Tektronix (former Synthesys Research)**
- **Strong IT Infrastructure**
  - **2 CAE/Compute Servers**

    IBM System x3650, Dual Intel Xeon Quad Core E5420

    IBM System x3650, Dual Intel Xeon Dual Core 5140
  - **2 Workflow/Workgroup Servers**

    IBM System x3650s, Dual Core Intel Xeon 5140, running Microsoft Windows Server 2003 R2, Sharepoint Services & Exchange 2007

Partnerships/Memberships

- **Hellenic Semiconductor Industry Association** member
  - http://www.hellenic-sia.org
- **Mi-cluster:** member to the **Corallia supported microelectronics cluster program**
  - http://www.corallia.org
- **Former IEEE P1901 Broadband over Powerline** working group member
  - http://grouper.ieee.org/groups/1901
- **Cadence Startup Accelerator Program** member
  - http://www.cadence.com/services/Pages/startup_accel.aspx
- **TSMC Europe Emerging Business Program (EBP)** member
- **IBM** Foundry Access through MOSIS

Why Analogies?

- Provides leading **analog/mixed-signal RF** silicon **Intellectual Property (IP) & design services**
  - Positioned in the Analog Mixed Signal, PHY & Physical IP market segments which are high demand and growth areas
- **High Speed analog/mixed-signal RF** and **FEC** silicon **design is still an art**
  - Analog IP blocks require tailored functionality, are not easily repeatable or programmable – FEC requires strong mathematical foundation and algorithmic understanding as well as HW implementation tradeoffs
  - Very **high speed analog PHY/RF** design remains **far from trivial**
- Analogies' **Intellectual Property** (IP) and **personnel's expertise** are its **key differentiators**
  - Based on innovative technologies that provide sustainable competitive advantage
  - Existing IP and team expertise an ideal fit for very high speed wireline & wireless RF interfaces, data communication and data storage applications, all deemed high growth markets

Thank you!

* Actual photo taken from the Analogies premises in Rio, Patras